



# FPGA DESIGN OF A CONTROLLER FOR SINGLE PHASE SCR CONVERTERS

## DESCRIPTION

Presented here is a design of an integrated circuit for a Universal **controller for single phase thyristor convertors**. The chip is designed in **VHDL** (Very High speed integrated Hardware Description Language and is implemented on an **FPGA** (Field Programmable Gate Array)

## FEATURES

- **Double buffered interface logic** allows configuration to **any bus width**, from **serial** to **parallel** of any width.
- Interface directly on a **dedicated data bus**, without bus interface logic, or on a **shared data bus**
- Instantiate the core as **stand-alone** or **cascaded**, in a daisy chain configuration.
- **Daisy chain multiple cores** on **one port address**.
- Instantaneous **phase angle** changes.
- Can be configured for any **oscillator frequency**.
- Can be configured for any **line frequency**.
- **Digital filtering** of **synchronizing input**.
- Configurable output **pulse width**
- Output pulse can be configured for a **train of pulses** or a **single pulse**.
- Can be configured for a **semi controlled bridge** or a **fully controlled bridge**.
- Implement a **dual bridge** for 4 quadrant control.

## APPLICATION

Thyristorised DC power control in a host of industrial and commercial applications:-

- 4-quadrant DC motor control in:-
  - Robotics
  - Industrial process equipment
- UPS battery chargers
- Lighting



## **VHDL Component Declaration:**

```
COMPONENT S_CON
  GENERIC (
    CASC          : INTEGER:=0;
    DBC           : INTEGER:=0;
    PWD           : INTEGER:=0;
    MCNT          : INTEGER:=2;
    MXC           : INTEGER:=0;
    OCB           : INTEGER:=1;
    LFRQ          : INTEGER:=1;
    TOPL          : INTEGER:=0;
    SEMI          : INTEGER:=0;
    OPN           : INTEGER:=0;
    BSW           : INTEGER:=1;
    C_LK          : INTEGER:=0;
    CON           : INTEGER:=1);
  PORT(
    OD            : IN      BUS1D(BSW-1 DOWNT0 0):=(OTHERS=>'0');
    OPR           : IN      BUS1D(NSL-1 DOWNT0 0):=(OTHERS=>'0');
    XG5           : IN      NODE:='0';
    CLKI          : IN      NODE:='0';
    RST           : IN      NODE:='0';
    CASI          : IN      NODE:='0';
    MAST          : IN      NODE:='0';
    FT            : BUFFER NODE;
    FU            : BUFFER NODE;
    CASO          : BUFFER NODE);
END COMPONENT;
```

## **FILES YOU GET**

i) FUNC.DOC	-	Documentation of functions & data types used in the core.
ii) README.DOC	-	Compile and licensing information.
iii) SCON.DOC	-	This document
a) MYLIB.VHD	-	PACKAGE
b) S_CON.VHD	-	TOP HIERARCHY DESIGN FILE
c) M_DFF.VHD	-	DESIGN FILE BELOW TOP HIERARCHY
d) S_DFF.VHD	-	-DO-
e) P_AD.VHD	-	-DO-
f) R_SL.VHD	-	-DO-
g) I_NCDEC.VHD	-	-DO-
h) U_DCNT.VHD	-	-DO-
i) A_DSB.VHD	-	-DO-
j) D_ECOT.VHD	-	-DO-
k) L_DRD.VHD	-	-DO-
h) D_BIL.VHD	-	-DO-
i) B_SHIFT.VHD	-	-DO-
j) S_TFF.VHD	-	-DO-
k) S_JKF.VHD	-	-DO-
l) F_DIV.VHD	-	-DO-
m) P_LSE.VHD	-	-DO-



## INTERFACE INFORMATION

Three types of interface schemes are described here viz Direct, Stand-alone and Cascaded. In the first there are no interface signals, and in both the other two schemes the data lines OD[],RST,CLKI can be shared with any number of peripherals. However the Chip Select line (OPR) must be unique for every core instantiated in the stand-alone scheme and common to all cascaded cores instantiated in the cascaded interface scheme.

### DIRECT CONNECTION

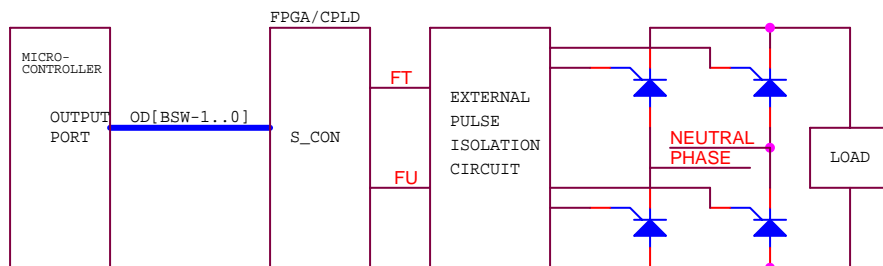
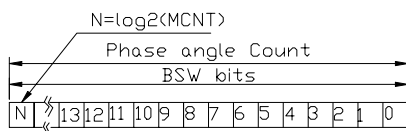


Fig 1

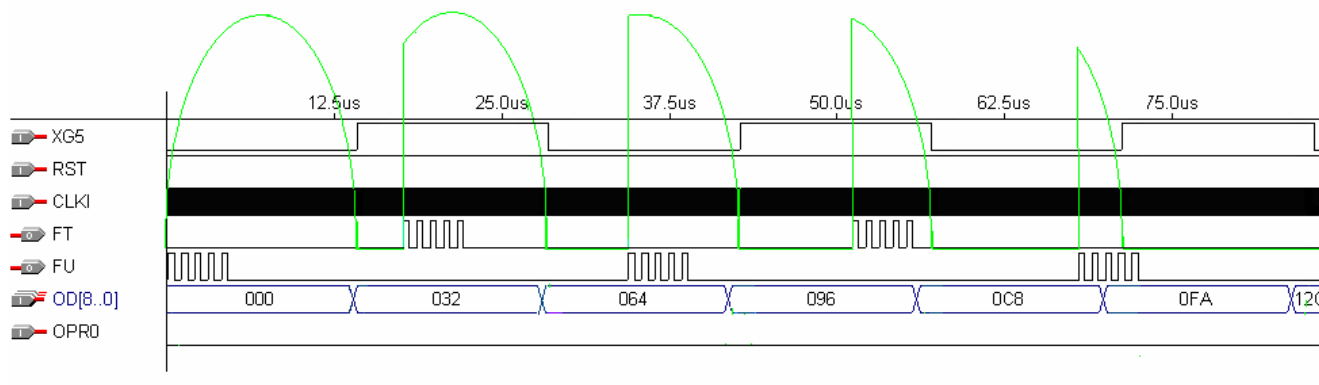
This option, selected by setting the OPN parameter to 0, will interface the internal or external CPU to a core, on one or more of its output ports. Data on the port is assumed to be always valid, thus eliminating the need for handshaked interface with the chip select input. Data transmission in this case is parallel and the number of port bits connected to the core must be able to accommodate the maximum data to be sent and is specified in the BSW parameter. This interface is indicated in situations where an instantaneous response is desired. As seen in the timing diagram below the core output changes as soon as the data on the bus changes.

### DATA WORD-fig 2



### TIMING -fig3

Figure shows 9 bits of data, 118H, being loaded using a 4 bit data bus  
OPN=0,BSW=9,MCNT=511





## INTERFACED CONNECTION

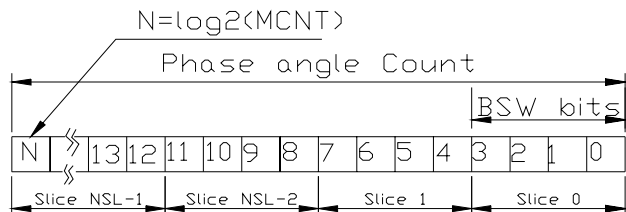
These interface schemes described hereunder require the OPN parameter to be set to 1.

The interface signals used here are described in the “**INPUT PORTS**” section

The data bus may be of any size from 1 bit serial, to parallel of any width. Its width is specified in the BSW parameter.

The data word required by the core is assembled internally from the sliced data it receives from the data lines. The width of the data word is specified in the MCNT parameter. The MSB slice will load first, LSB will load last. A complete write cycle requires all the slices (NSL) required for the data word must be sent contiguously. This comprises the full write cycle, which must be repeated everytime data is to be written to the core.

### DATA WORD-fig 4



$NSL = \text{Number of slices of data the CPU needs to send} = \lceil \log_2(MCNT) + 1 \rceil / BSW$

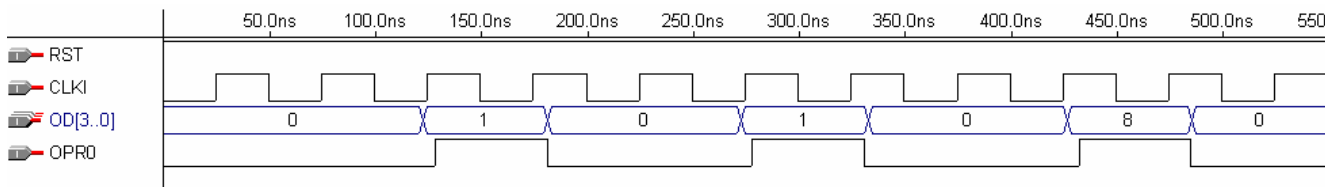
If the result of division has a remainder, add 1 to the result

The function LOG2() returns the upper index of an array required to hold a number, thus LOG2(7)=2

### fig 5a OPR TIMING-SLICED DATA

Figure shows 9 bits of data, 118H, being loaded using a 4 bit data bus

OPN=1,BSW=4,MCNT=511,NSL=3



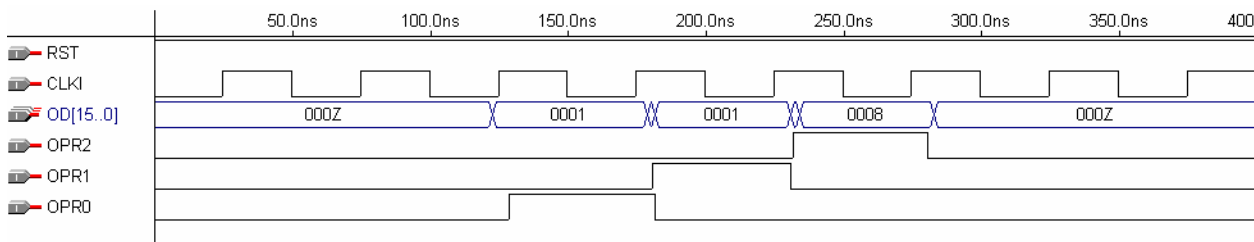
### TIMING REQUIREMENTS

- Frequency of OPR  $\leq 1/3$  of CLKI
- Hi time of OPR  $\geq 1$  CLKI
- Lo time of OPR  $\geq 1$  CLKI

### fig 5b OPR TIMING-UNSLICED DATA

Figure shows 16 bits of data, 0118H, being loaded using a 16 bit data bus, onto 3 stand-alone cores

OPN=1,BSW=16,MCNT=65535, NSL=1

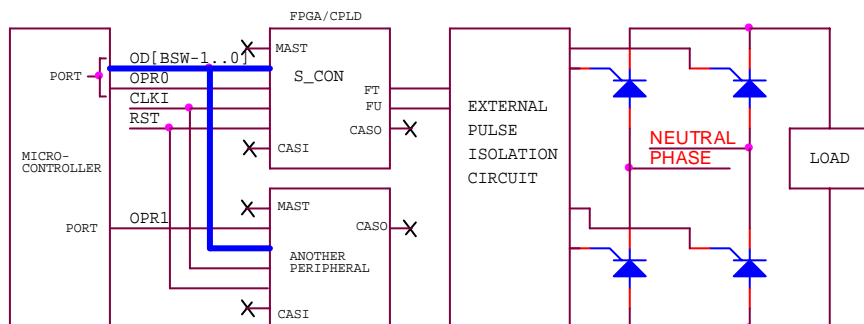


### TIMING REQUIREMENTS

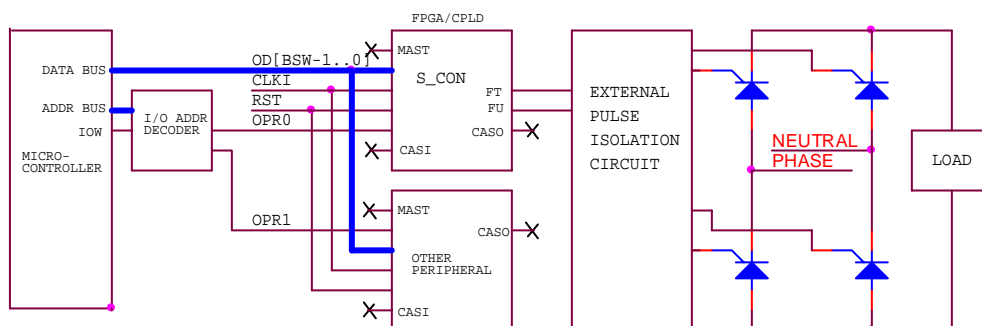
- Each OPR[] input may come back to back one after the other with no gap in between.
- Hi time of each OPR[] input  $\geq 1$  CLKI.



## STAND-ALONE INTERFACE – SHARED PORT



## STAND-ALONE INTERFACE – SHARED BUS



This option is enabled by setting the CASC parameter to zero, the MAST and CASI inputs are unused and may be connected to any constant.

This scheme will interface the core to an internal or external CPU with a separate chip select for each core instantiated on the common data bus. Chip-select signals can be generated either by an i/o address decoder, within the PLD or from an output port on a micro-controller. Each chip select line brings along not only a logic overhead and additional pinouts but also the advantage of random access.

In this scheme the core is ready to accept data soon after RST=1. The core with an active OPR signal will accept data and only one core at a time must be activated. The calculation of number of slices(NSL) and structure of the data word to be sent by the controller are shown above. The timing constraints for sending each data slice to the core are shown in fig 5. After a core receives all the entire data word, it initializes the data load logic to the first slice.

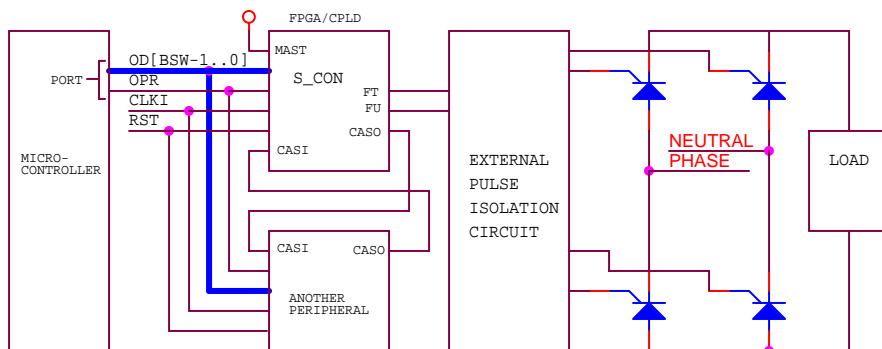


## CASCADED INTERFACE

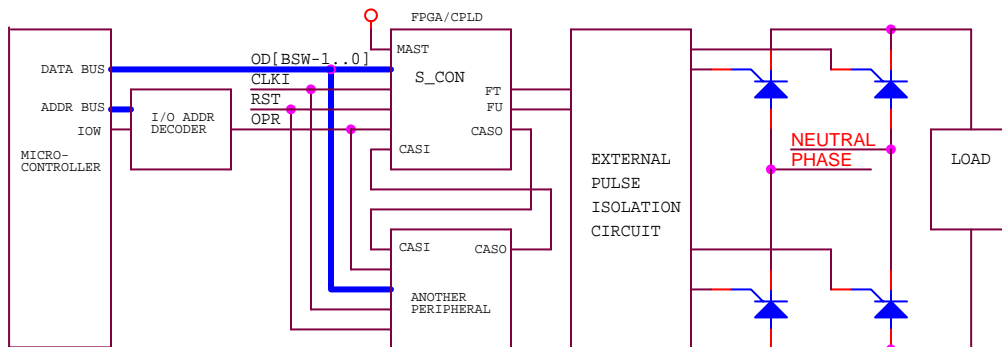
This option is enabled by setting the CASC parameter to one and connecting the MAST input of the first core in the chain to '1' and the CASO output of each core to the CASI input of the next core in the chain. The CASO output of the last core in the chain is connected to the CASI input of the master, or the first core in the chain.

This interface option will interface an internal or external CPU to all cores, instantiated on the common data bus, with a single chip select. Although the chip select logic overhead is minimum in this case, the cores cannot be accessed randomly and must be accessed sequentially one after the other and the entire sequence must be completed everytime, a process known as daisy chaining. The core, configured as the master will load first followed by the next in the chain. After a core receives its data, it pulses the CASO output, which being connected to the next core in the chain, enables it for data reception. After all the cores in the chain are loaded, the master is once again enabled.

## CASCADED INTERFACE - SHARED PORT



## CASCADED INTERFACE - SHARED BUS





## INPUT PORTS

NAME	DESCRIPTION	WIDTH	DESCRIPTION
OD	Data bus	BSW	Data bus
CLKI	Clock	1	Positive edge triggered clock. Synchronizes all internal operations
RST	Reset	1	Asynchronous, active lo, resets all internal logic
XG5	Line sync	1	Line synchronizing signal
OPR	Chip select	1	Active hi, enables the internal data load logic. Must be synchronous to the rising or falling edge of the CLKI input. Data latches internally at the first rising edge of CLKI after OPR goes Hi. Only used when OPN<>0 See “ <b>INTERFACE INFORMATION</b> ” for timing constraints
CASI	Cascade in	1	If the core is in a cascaded configuration(CASC=1) and is not the master, connect CASI to CASO of the previous core in the chain, if it is the master, set it to CASO of the last core in the chain. In a stand-alone configuration(CASC=0) it is unused and may be left open.
MAST	Master select	1	When the core is a master in a cascaded configuration(CASC=1), set MAST to Hi. In a cascaded configuration if it is not the master, set it Lo. In a stand-alone configuration(CASC=0), it is unused and may be left open.

## OUTPUT PORTS

NAME	DESCRIPTION	COMMENTS
FT	SCR gate pulse(quadrant-1)	Appears when phase count crosses sawtooth ramp
FU	SCR gate pulse(quadrant-2)	Appears when phase count crosses sawtooth ramp.Unused when SEMI=1
CASO	Cascade out	Used in a cascaded configuration (CASC=1), to enable the next core in the chain for data loading from the data bus. In a stand-alone configuration, it is unused and drives out Lo.

## PARAMETERS-All values of INTEGER type

NAME	MIN	DESCRIPTION
CASC	0	Core is Cascaded/Standalone –1/0. Determines the behaviour of MAST and CASI inputs and the CASO output.
DBC	0	Latency count for filtering the XG5 input. Keep as low as possible to prevent excessive delay.
PWD	0	Width, in micro-seconds, of the FT & FU output pulses
MCNT	2	Phase angle count corresponding to 180 deg (SEMI=1) or 360 deg (SEMI=0). Determines the BSW and NSL parameters
MXC	0	Period, in micro-seconds, of each pulse, in the train of pulses at the output (when TOPL=1)
OCB	1	Frequency of internal clock for output pulse duration (determines the width accuracy of the output pulses). Also used to equalize the Hi and Lo periods of the XG5 input
LFRQ	1	Frequency in hertz, of mains voltage and the XG5 input
TOPL	0	When TOPL=1 the outputs, FT and FU are a Train Of Pulses, with a 50% duty. When TOPL=0 the outputs, FT and FU are a single pulse.
BSW	1	Width of the OD[] input port. When OPN=0, BSW>=LOG2(MCNT)+1
C_LK	0	Frequency of the CLKI input.
CON	1	Reserved keep unused
SEMI	0	Semi controlled bridge (SEMI=1) or fully controlled (SEMI=0).
OPN	0	Bus interface option. See section on “ <b>INTERFACE INFORMATION</b> ” above



## SUGGESTED PARAMETER VALUES FOR 50Hz LINE FREQUENCY

```
DBC=50          --FILTER COUNT FOR SYNC I/P
PWD=660         --O/P PULSE WIDTH IN MICRO SECS
MCNT=65535     --MAX COUNT FOR 10ms(SEMI=1)/20ms(SEMI=0)
MXC=51         --PERIOD, IN  $\mu$ s OF EACH PULSE IN THE O/P TRAIN OF PULSES
OCB=5000       --FREQ OF CLK FOR O/P PULSE WIDTH & 1/2 SYNC PULSE WIDTH
LFRQ=50        --LINE FREQ(Hz)
TOPL=0         --TRAIN OF PULSES LOGIC ENABLED/DISABLED(1/0)
SEMI=1         --SEMI/FULL CONTROLLED BRIDGE (1/0)
OPN=1          --BUS INTERFACE 0(NONE), 1(INTERNAL), 2(EXTERNAL)
BSW=16         --DATA BUS WIDTH
C_LK=20000000, --GLOBAL CLK FREQ
CON=1          --CONVERTER USED/NOT
```

## SAMPLE DESIGN (1)

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(
    OD          :IN      BUS1D(15 DOWNT0 0):=(OTHERS=>'0');
    OPR         :IN      BUS1D(15 DOWNT0 0):=(OTHERS=>'0');
    XG5         :IN      NODE:='0';
    CLKI        :IN      NODE:='0';
    RST         :IN      NODE:='0';
    FT          :BUFFER  NODE;
    FU          :BUFFER  NODE;
  );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

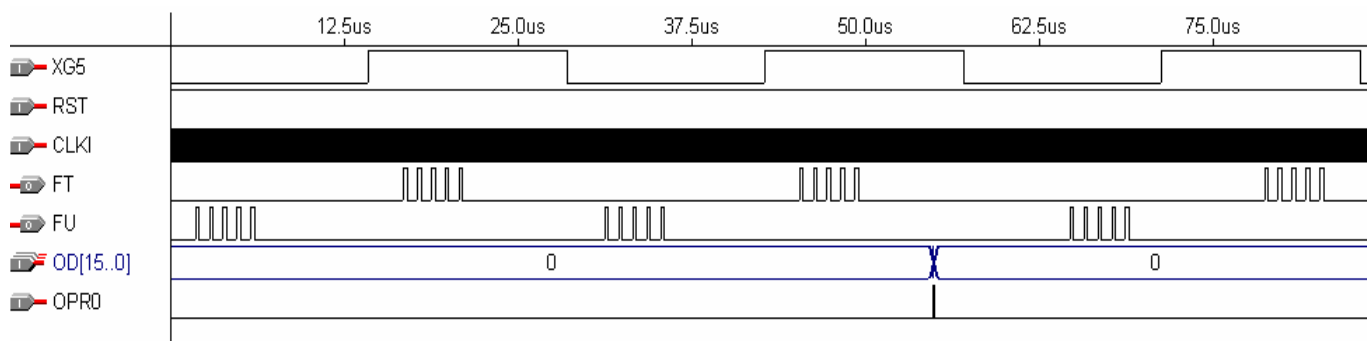
SIGNAL CASO :NODE;
BEGIN

A1: S_CON GENERIC MAP (
  CASC=>0,
  DBC=>0,
  PWD=>5,
  MCNT=>127,
  MXC=>1,
  OCB=>1000000,
  LFRQ=>35000,
  TOPL=>1,
  SEMI=>0,
  OPN=>1,
  BSW=>16,
  C_LK=>20000000,
  CON=>1
)
PORT MAP (OD(15 DOWNT0 0),OPR(0),XG5,CLKI,RST,CASO,'0',FT,FU,CASO);

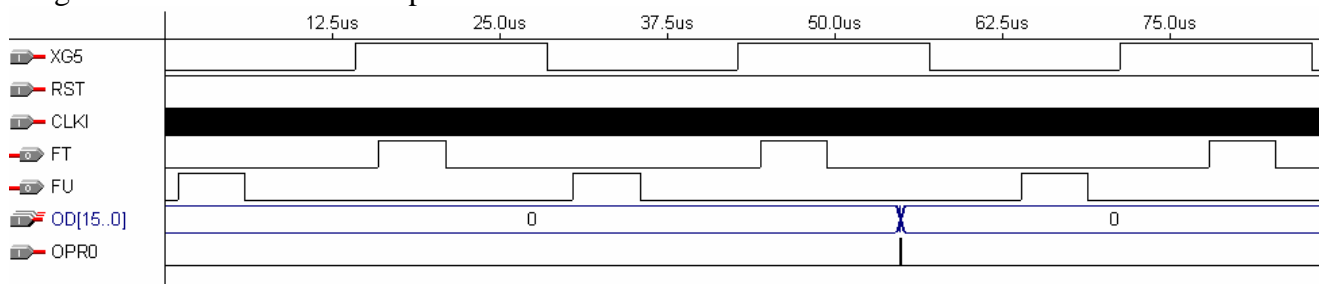
END MYTOP;
```



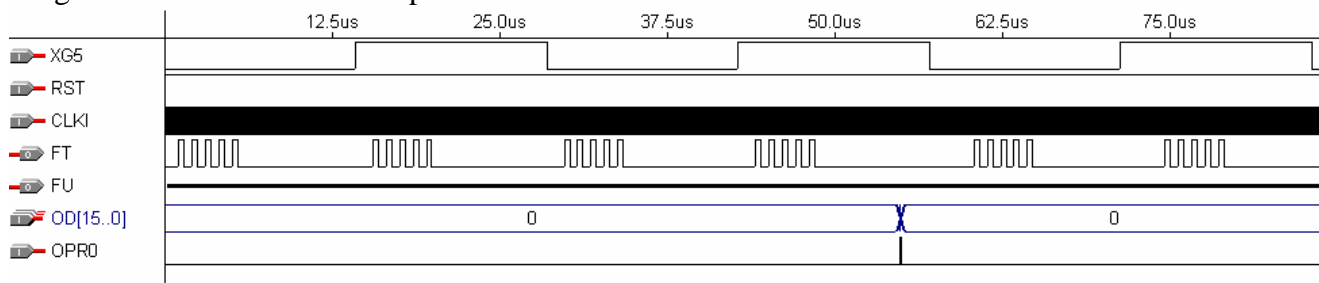
## TIMING DIAGRAM – SAMPLE DESIGN



Program is same as above except TOPL=0



Program is same as above except SEMI=1



Expanded view of OPR0 and OD[] in the above timing diagrams

